COMPILATION IN A HIGH-LEVEL MODELING SYSTEM

ABSTRACT

Methods and apparatus are disclosed for compiling high-level blocks of an electronic hardware design in a high-level modeling system (HLMS) into hardware description language (HDL) components. Clock requirements are established, along with (optionally) explicit connections from implicit connections between the high-level blocks. In one pass through the high-level blocks, HDL components are generated that are consistent with the clock requirements and explicit connections, if any.